Compact 10-Gbit/s Optical Transmitter and Receiver Circuit Packs

Yukio Kobayashi, *Member, IEEE,* Yuji Akatsu, Kiyoski Nakagawa, *Senior Member, IEEE,* Hiroyuki Kikuchi, *Member, IEEE,* and Yuhki Imai, *Member, IEEE*

Abstract—**Compact wideband 10-Gbit/s optical transmitter and receiver circuit packs are realized using high speed analog and digital GaAs IC's as well as a highly thermally conductive board and appropriately designed small function block modules that employ multichip packaging and resonant cavity mode damping. To achieve a compact receiver, the receiver circuit employs a clamp and peak-detector IC in the high speed analog equalizer amplifier to obtain a constant output direct current level for any mark density imbalance in the number of ones and zeros in the signal and a variable phase-shifter IC in the timing circuit. Realized circuit pack size is 200 ×280 × 15.24 mm and the power consumption of each pack is about 25W.**

I. Introduction

SINCE the ITU recommendations on synchronous digital hierarchy (SDH) were published in 1988 [1], SDH-based transmission systems up to 2.5 Gbit/s (STM-N; N =1, 4, 16) and SONET transmission systems (STS-N and OC-N; N =1, 3, 9, 12, 18, 24, 36, 48) in the U.S. digital transmission hierarchy [2] have been developed. For broadband ISDN and multimedia services, transmission system capacities of tens or hundreds of gigabits per second are needed. One step toward this goal is the development of high-speed semiconductor devices [3], [4]. In addition, for multigigabit per second fiber optic links, compact circuit packs are strongly demanded.

In this paper, we present a newly developed compact 10 Gbit/s optical transmitter circuit pack (TX CP) and a companion receiver circuit pack (RX CP). Both packs are composed of small function block modules created with high speed analog GaAs IC's [5]–[7], digital IC's reported in [6], multichip packaging technology, resonant cavity mode damping technology, and highly thermally conductive boards. To achieve a compact receiver, the receiver circuit employs a clamp and peak-detector IC in the high speed analog equalizer amplifier to obtain a constant output dc level in the case of a mark density imbalance in the number of ones and zeros at the section over head (SOH) bytes [8] or at the payload area where the bytes are sometimes consecutive identical digits, and a variable phase-shifter IC in the timing circuit. The circuit packs are 200 × 280 × 15.24 mm in size with a power consumption of about 25 W per pack.

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Y. Kobayashi, Y. Akatsu, and K. Nakagawa are with Lightwave Communication Laboratory, NTT Optical Network Systems Laboratories, Kanagawa 283-03, Japan.

H. Kikuchi is with NTT Electronics Technology Corp., Kanagawa 24301, Japan.

Y. Imai is with NTT LSI Laboratories, Kanagawa 243-01, Japan.

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Section II outlines the circuit packs and Section III explains the circuit design. Focus is placed on a newly designed clamp and peak-detection circuit and a phase shifter circuit. Finally, Section IV describes the performance of the circuits and the circuit packs.

II. Module Structure

Taking ITU SDH recommendations [1], the application area, and current device feasibility into account, the circuit pack (CP) interface for the high speed side (transmission line side) was set at a 10-Gbit/s single mode optical NRZ signal, i.e., SDH level of STM-64 or OC-192 in SONET, and the interface for the low speed side was set at a 1.25 Gbit/s electrical signals. The low speed side bit rate of 1.25 Gbit/s was decided by taking into account the byte interleave multiplexing scheme reported in [9], and versatility of the employed IC's.

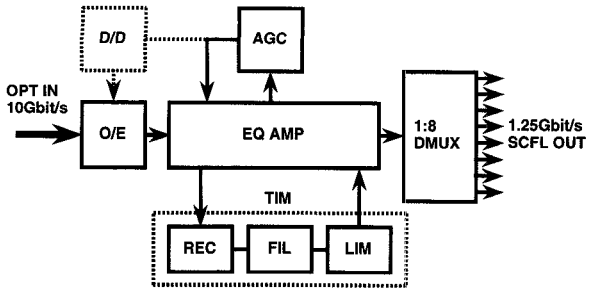
To meet NTT standards for cabinet size and allowable power consumption, the size of the TX and RX CP's was determined as 200 × 280 × 15.25 mm and the total power consumption per CP was limited to about 25 W with forced air cooling.

For design and development, we divided the CP's into three categorized areas: circuit pack boards, small function block modules (SFB) installed on the circuit pack boards, and devices used. Another design goal was that SFB characteristics should be measured stand-alone and they were versatile enough to suit any circuit pack. For the circuit pack board design, SFB allocation was studied from the view point of power dissipation and noise characteristics. The base material of the board was aluminum. To reduce the resonance cavity modes caused by packaging, a microwave absorber [10] was attached to the back side of the module cover. IC's in the SFB's were mounted on a metal plate by silver paste epoxy for high thermal conductivity and assembled into SFB packages.

III. Circuit Design

A. Receiver Circuit Pack

The receiver CP consists of an optical-to-electrical conversion (O/E) module, an equalizer amplifier (EQ AMP) module which includes a decision circuit, a timing extraction (TIM) module, a 1:8 demultiplexing (DMUX) module, and an automatic gain control (AGC) module as shown in Fig. 1. A dc (direct current) to dc conversion (D/D) circuit would be used when an avalanche photo-diode (APD) detector is employed in the O/E module. When a PIN photo-diode (PIN-PD) is employed, an appropriate bias voltage for the PIN-PD,



Note Bold box indicates the small function block (SFB) modules
AGC and D/D are composed of discrete components

AGC:	Automatic Gain Control
D/D	DC to DC Converter
DMUX	Demultiplexer
EQ AMP	Equalizer Amplifier
FIL	Filter
LIM:	Limiter
OPT	Optical Signal
O/E	Optical to Electrical Converter
REC:	Rectifier
SCFL	Source Coupled FET Logic
TIM.	Timing Circuit

Fig. 1. Receiver circuit pack block diagram.

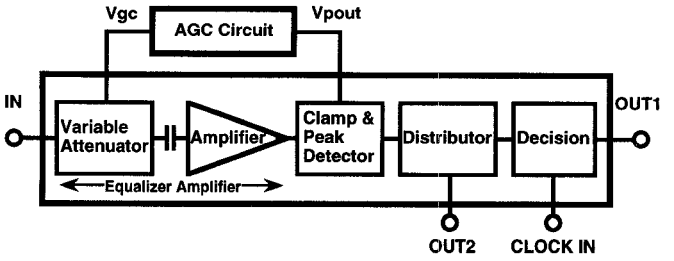


Fig. 2. Equalizer amplifier block diagram.

for instance 5 V, is applied directly from one of the IC power supplies.

In the DMUX block, the 10-Gbit/s signal is demultiplexed to eight 1.25-Gbit/s source coupled FET logic (SCFL) signals. [5] The DMUX block consists of one 1:2 DMUX IC and a dual 1:4 DMUX IC for demultiplexing a 10 Gbit/s signal to eight 1.25 Gbit/s signals, and an 8 channel D-type flip-flop (DFF) IC which reshapes the eight 1.25 Gbit/s signals. [9]

The O/E module consists of a PIN-PD or an InGaAsP/InAlAs APD and a GaAs transimpedance amplifier IC. [11]

Fig. 2 shows the block diagram of the EQ AMP module. It is composed of a variable attenuator IC, two amplifier IC's, a clamp and peak-detector IC, a distributor IC, and a decision IC. The variable attenuator and amplifier IC's were connected via a capacitor of about 22000 pF. These IC's operate as an equalizer amplifier with gain of about 30 dB and a 20 dB gain-control range. The variable attenuator IC uses FET's as variable resistors [6]. Because of the coupling capacitor in the equalizer amplifier, the dc level can be varied for any mark density imbalance in the number of ones and zeros. Thus clamping the signal was necessary to obtain a constant output dc level. A peak detector was also required to achieve the AGC function in combination with the variable attenuator.

We integrated the clamp and peak-detector function in a one-chip IC. The circuit diagram of the IC is shown in Fig. 3. It consists of a clamp circuit (diode D1 and capacitor C1), a peak-detector circuit (diode D2 and capacitor C2), and an input matching circuit, and output buffers. The output voltage

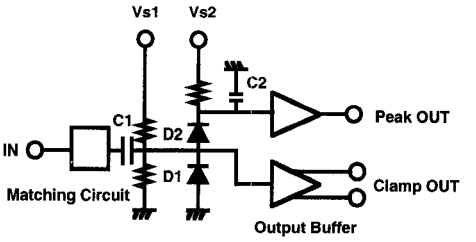
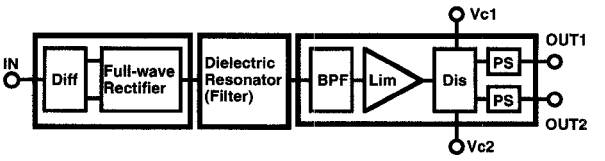


Fig. 3. Schematic of clamp and peak detector IC.



(Note) PS: Phase Shifter
Diff: Differentiator
Dis: Distributor
Lim: Limiter Amplifier

Fig. 4. Timing extraction block diagram.

was designed to be clamped to the source-coupled FET logic (SCFL) level [5]. Diode gate sizes are 3 μm x 25 μm for D1 and D2. Capacitors $C1$ and $C2$ are 20 pF and 10 pF, respectively.

The distributor IC has the role of distributing the signal to the decision IC and the TIM module [12]. An AGC circuit was installed between the peak-detector output port V(pout) and variable-attenuator control port (Vgc).

Fig. 4 shows the block diagram of the TIM module. It consists of a dielectric resonator, a band-pass filter, three limiter IC's, a distributor IC, two variable phase shifter IC's, a differentiator IC and a full-wave rectifier IC. The differentiator and rectifier IC's extract the clock signal from the input data signal. The differentiator IC uses a $\lambda/4$ (a quarter wavelength) meandering coplanar-waveguide short stub with input and output buffers [7]. The rectifier employs a Gilbert cell with input and output buffers [7]. A high-Q dielectric resonator with a Q factor value of about 1000 was used for a timing tank. The limiter has a narrow-band MMIC configuration to maintain a constant output power with low phase deviation over a wide dynamic input range [7]. The limiter IC's were cascaded to obtain the high gain of 60 dB.

The distributor IC provides clock signals to the EQ AMP and DMUX modules. The variable phase shifter IC has a function of adjusting the clock signal phase for the EQ AMP and DMUX modules. It is indispensable in realizing a compact receiver, because the conventional phase shifter is very bulky and fine phase adjustment between data and clock signals by means of cable length adjustment is necessary for the decision circuit.

Fig. 5 shows the schematic circuit of the variable phase shifter. It is composed of an attenuator, an analog phase shifter, and an amplifier. The phase shifter is a reflection-type circuit with a reduced-size branch-line hybrid and diodes as variable capacitors. For the reduced-size branch-line hybrid, a uniplanar structure was employed [12]. The attenuator and amplifier were used to maintain a large phase-control range even with large input signals. The attenuator makes the internal signal of the diode small enough to realize the large variable-capacitance

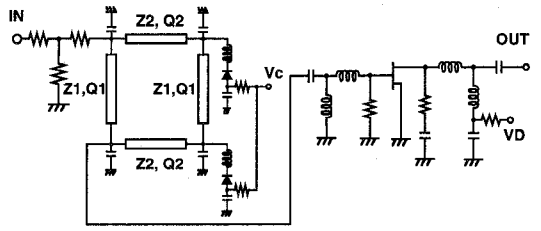
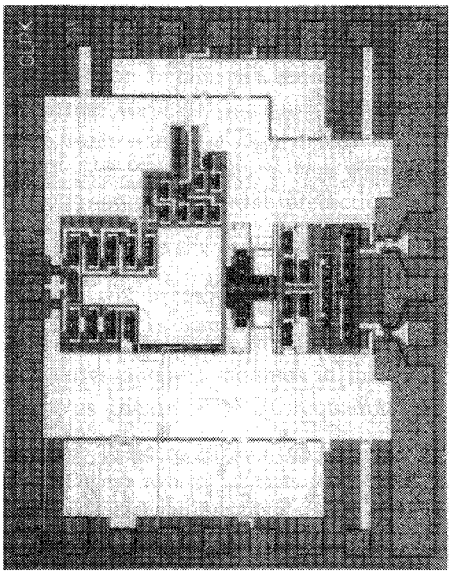
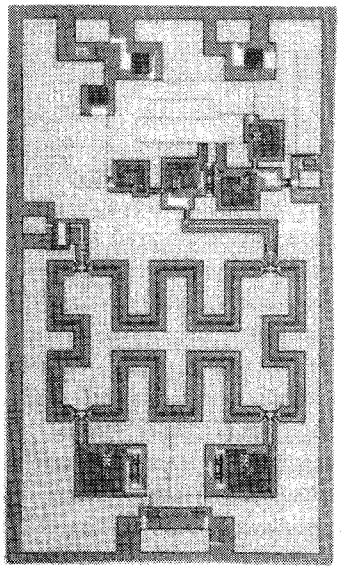


Fig. 5. Schematic of phase shifter circuit.



(a)



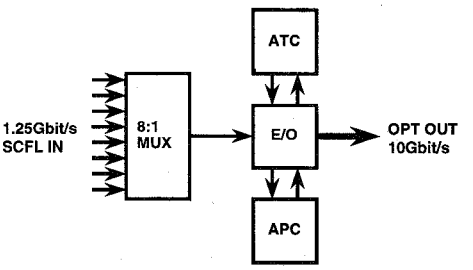
(b)

Fig. 6. Microphotographs of IC's. (a) Clamp and peak detector. (b) Variable phase shifter.

range needed for large phase shifts. The amplifier compensates the losses induced by the attenuator and hybrid. The amount of the phase shift is determined by adjusting the control voltage ($Vc1$ and $Vc2$) manually when the decision circuit is installed and the phase shift is measured at the optimum decision timing.

All IC's were fabricated by NTT Electronic Technology Corporation using self-aligned ion implantation and $n+$ layer technology [3], [4]. The gate length was 0.2 μm; f_T and $f_{\max}$ were 40–50 GHz and 60–70 GHz, respectively. After the IC's passed on-wafer testing, they were encased in metal-based packages and ceramic packages. Fig. 6 shows microphotographs of a clamp and peak detector IC, and a variable phase shifter IC. Chip size is 2 x 2.5 mm and 1.58 x 2.5 mm, respectively.

The power consumption of the O/E, EQ AMP, TIM, AGC, and DMUX modules were estimated to be about 1W, 8W, 5W, 1W, and 10W, respectively.



Note: Bold box indicates the small function block (SFB) modules.
ATC and APC are composed of discrete components.
APC: Automatic Power Control
ATC: Automatic Temperature Control
E/O: Electrical to Optical Converter
MUX: Multiplexer
OPT: Optical Source Signal
SCFL: Source Coupled FET Logic

Fig. 7. Transmitter circuit pack block diagram.

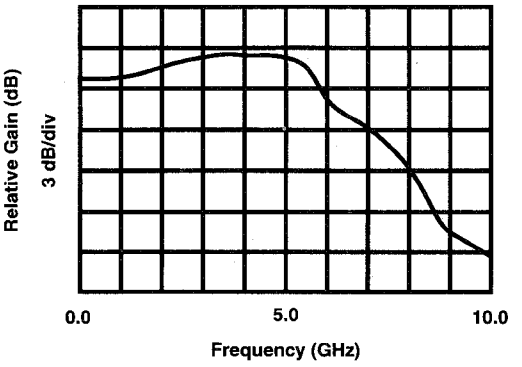


Fig. 8. Frequency characteristics of O/E module.

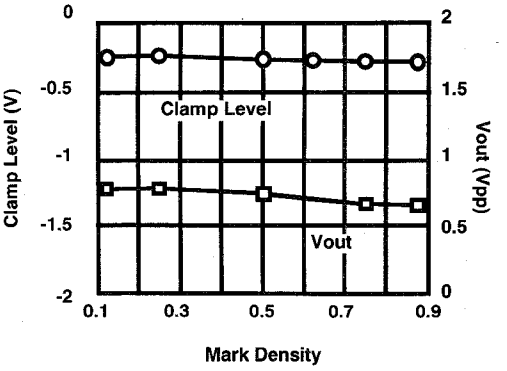


Fig. 9. Mark density dependence of clamp level and output voltage amplitude.

B. Transmitter Circuit Pack

The TX CP consists of an electrical to optical conversion (E/O) module, a multiplexing (MUX) module, an automatic

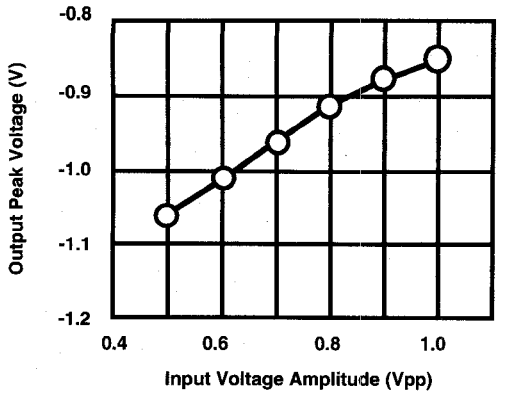


Fig. 10. Peak detector output voltage versus input voltage amplitude.

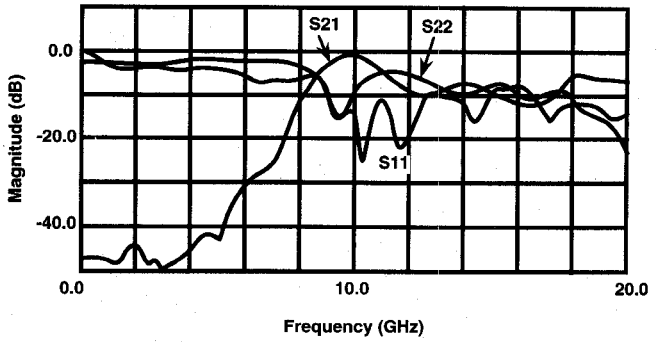


Fig. 11. Frequency characteristics of the variable phase shifter.

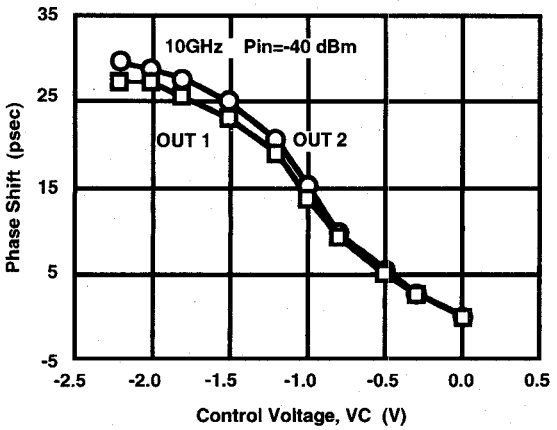


Fig. 12. Phase shift versus control voltage for TIM module.

power controller (APC) module, and a temperature control (ATC) module as shown in Fig. 7. A direct laser diode (LD) modulation module was employed for its compactness and versatility, although an external optical signal modulation module could also be applied.

The E/O module consists of a strained MQW DFB-LD, a GaAs MESFET driver IC [13], [14], and a temperature controller. Two types of modules were developed for the wavelengths of 1.3 μm and 1.55 μm.

In the MUX module, eight 1.25 Gbit/s SCFL signals are multiplexed to yield the 10 Gbit/s SCFL signal. The MUX module consists of an 8-channel D-type Flip-Flop (DFF) IC which reshapes the eight 1.25 Gbit/s input signals, a dual 4:1 MUX IC, and a 2:1 MUX IC for multiplexing 1.25 Gbit/s signals to a 10 Gbit/s signal [8].

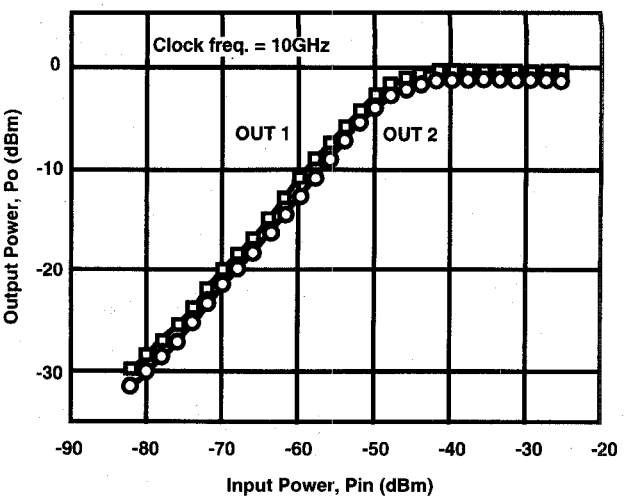


Fig. 13. Output power versus input power for TIM module.

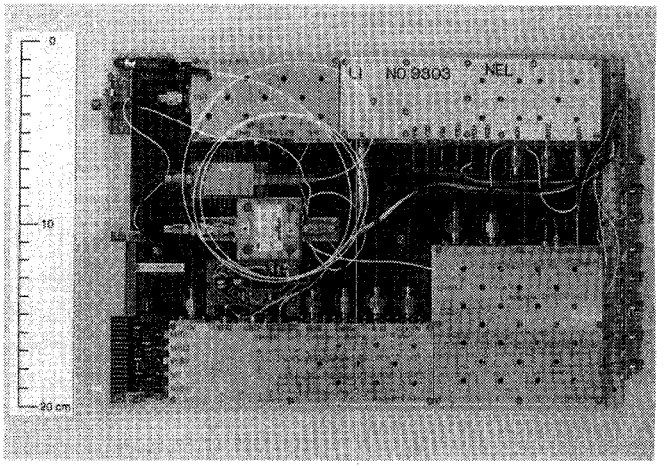


Fig. 14. Receiver circuit pack.

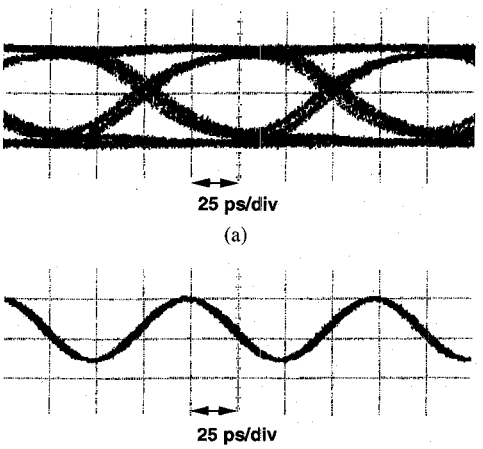


Fig. 15. EQ AMP and TIM module output signals. (a) Equalizer output signal. (b) Timing output signal.

The power consumption of the E/O, ATC, APC, and MUX modules was estimated to be about 4, 8, 1, and 10 W, respectively.

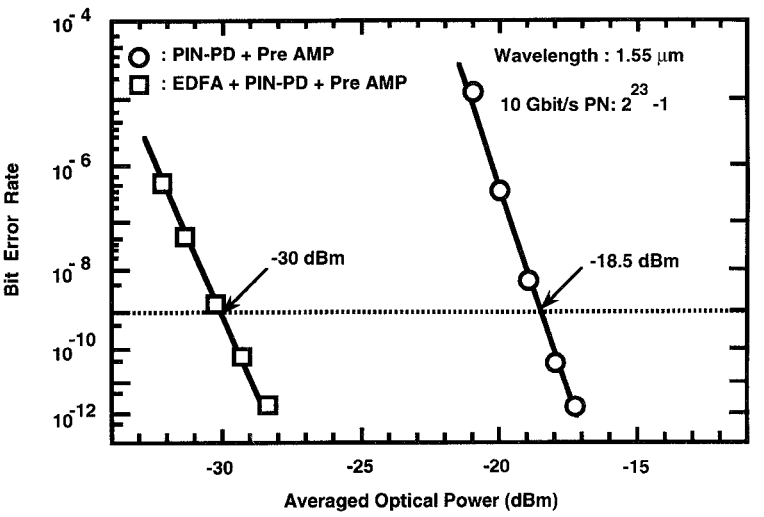


Fig. 16. Measured bit error rate characteristics.

IV. Performance

A. Receiver Circuit Pack

Fig. 8 shows the frequency characteristics of the O/E module as measured by an optical component analyzer; the 3-dB bandwidth was about 7 GHz.

Maximum gain of the realized EQ AMP was 33 dB with a 3-dB bandwidth of 9 GHz. The gain was controlled from 13 dB to 33 dB without any frequency performance degradation.

The clamp and peak-detector performance for the EQ AMP module is shown in Figs. 9 and 10. Fig. 9 shows the mark-density dependencies of the clamp level and output-voltage amplitude. The input signal was a 10 Gbit/s NRZ 2^{23}-1 pseudo random signal with 1 V_{pp} amplitude from a pattern generator. The clamp level and output voltage amplitude were maintained at around 0.25 V and 0.75 V_{pp}, respectively, while the mark density varied from 0.1 to 0.9. A plot of the peak-detector output voltage versus input voltage amplitude is shown in Fig. 10. Good linearity and high output-to-input voltage ratio were obtained. In combination with the equalizer amplifier, this level of performance is enough to assure adequate automatic gain control operation.

Frequency characteristics of the variable phase shifter IC for the TIM module are shown in Fig. 11. S_{21}, S_{11}, and S_{22} were -0.5, -15, and -8 dB at 10 GHz, respectively. The changes in S_{21}, S_{11}, and S_{22} at 10 GHz were very small when the phase shift was changed by the control voltage (VC). A plot of the phase shift versus the control voltage for the TIM module is shown in Fig. 12. The module input power was -40 dBm. The range of the phase shift was 30 ps at 10 GHz for voltages from 0 to -2 V. The input power dependency of the output power at 10 GHz for the TIM module is shown in Fig. 13. The module achieved a wide range operation with inputs from -80 to -25 dBm; a linear gain region from -80 to -45 dBm and a saturated output power region from -45 to -25 dBm.

The fabricated receiver circuit board is shown in Fig. 14. The TIM module uses a microwave absorber attached to the back side of the module cover to suppress the resonance cavity modes.

Prototype CP's were fabricated and tested. To measure receiver sensitivity precisely, an optical signal generated by a $LiNbO_3$ Mach-Zehnder external modulator with a continuous wave (CW) laser diode at the wavelength of 1.55 μm was used. Fig. 15(a) shows the EQ AMP output with the PIN-PD module and Fig. 15(b) shows the timing circuit block output for a 10 Gbit/s NRZ 2^{23}-1 pseudo random signal. The measured bit error rate characteristics using a 10^{23}-1 pseudo random signal without and with an Erbium-Doped fiber amplifier (EDFA) pumped by a 1.48 μm LD are shown in Fig. 16. The measured receiver sensitivities were -30 dBm with an EDFA and of -18.5 dBm without an EDFA.

In combination with an EDFA and a PIN-PD, the RX CP can be used for long haul transmission systems. With just a PIN-PD or an APD-PD, the RX CP can be used for short haul transmission systems.

B. Transmitter Circuit Pack

The fabricated transmitter circuit board is shown in Fig. 17. The optical output powers were about $+2.0$ dBm for 1.3 μm and $+0.5$ dBm for 1.55 μm for a 10 Gbit/s NRZ $2^{23}-1$ pseudo random signal. Fig. 18(a) shows the MUX output signal wave form before injection into the LD driver circuit. Fig. 18(b) shows the 1.55 μm optical output signal pattern. Jitter of about 10 ps was observed because there is some impedance mismatch between the drive IC and DFB-LD. Further study is still needed to understand and minimize this phenomena.

V. Conclusion

To develop multigigabit per second optical interface circuit packs that can be used for microwave and optical transmission, we have developed compact wideband transmitter and receiver circuit packs that are composed of small function block modules. The small function block modules can also be used in several other application areas. One small function block, the EQ AMP, employs a newly fabricated clamp and peak-detection IC and a variable phase shifter IC to obtain a constant

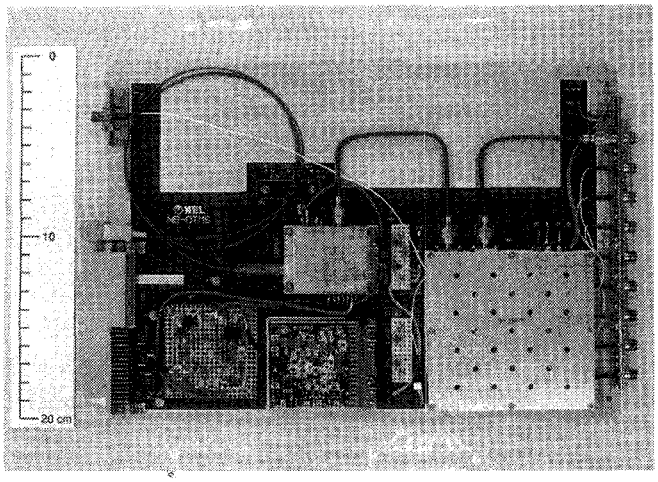


Fig. 17. Transmitter circuit pack.

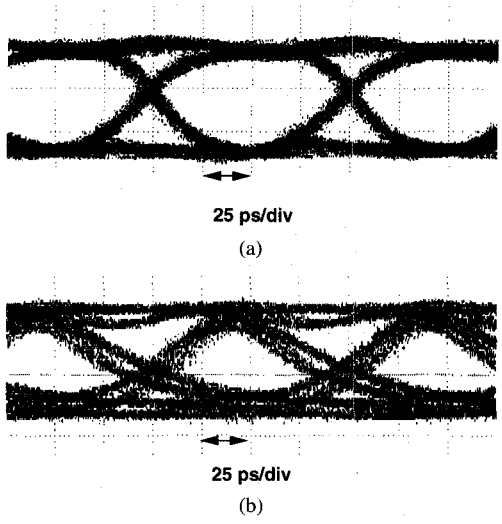


Fig. 18. MUX and E/O module output signals. (a) Multiplexer output signal. (b) 1.55 μm optical output signal.

output dc level for any mark density imbalance in the number of ones and zeros. The fabricated transmitter and receiver circuit packs are about 200 × 280 × 15.25 mm in size and each circuit pack consumes about 25 W.

The receiver sensitivities of −30 dBm with an Erbium-Doped fiber amplifier and −18.5 dBm without fiber amplifier were achieved at the wavelength of 1.55 μm for a 10 Gbit/s NRZ $2^{23}-1$ pseudo random signal.

The optical output power of the transmitter CP's was about +2.0 dBm for 1.3 μm and +0.5 dBm for 1.55 μm for a 10 Gbit/s NRZ $2^{23}-1$ pseudo random signal.

According to these results, we have confirmed that the small function block modules, the transmitter circuit packs and the receiver circuit packs are useful and feasible for 10 Gbit/s transmission systems.

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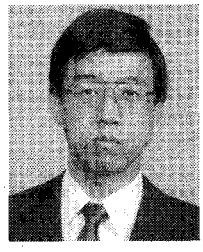
Yukio Kobayashi (M'79) received the B.E. and M.E. degrees in electrical engineering from Nagoya University in 1971 and 1973, respectively.

He joined NTT Electrical Communication Laboratories in 1973, and engaged in the research and development of undersea cable transmission systems and optical trunk transmission systems. Since 1988 he has been engaged in the design and development of SDH (SONET) optical transmission systems. He is presently working on 10 Gbit/s optical transmission systems.

Mr. Kobayashi is a member of the Institute of Electronics, Information and Communications Engineers of Japan.



Yuji Akatsu was born in Hokkaido, Japan, on Nov. 16, 1960. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hokkaido University, Sapporo, Japan, in 1983, 1985, and 1988, respectively.

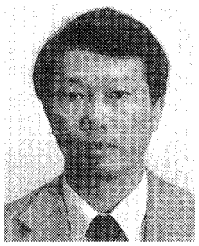
In 1988, he joined NTT Opto-Electronics Laboratories, Atsugi, Kanagawa, Japan, and was engaged in research on MOMBE and MOVPE growth for opto-electronic devices. Since 1990, he has been engaged in research on high speed receiver OEIC's, optical modules, and high speed photodetectors, for optical communication systems.

Dr. Akatsu is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan and the Japan Society of Applied Physics.

Kiyoski Nakagawa (SM'91) received the B.E., M.E., and Dr.E. degrees in electrical communication engineering from Osaka University, Japan, in 1968, 1970, and 1980, respectively.

He joined the Electrical Communication Laboratory, NTT, in 1970. From 1970 to 1974, he was engaged in the research and development of millimeter waveguide transmission systems. Since 1975, he has been engaged in research and development of high-speed optical fiber transmission systems. Presently, he leads the Optical Communications Systems Research Group, NTT Optical Network Systems Laboratories.

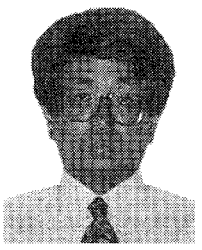
Dr. Nakagawa received the 1983 and 1990 Distinguished Achievement Awards from the Institute of Electronics Information and Communication Engineers of Japan, the 1978 Electronics Letters Premium, and the 1989/1990 Oliver Lodge Premium from the IEE, and the 1994 Maejima Award from the PTT Association.



Hiroyuki Kikuchi (M'89) was born in Tokyo, Japan, on Apr. 28, 1948. He received the B.S. and M.S. degrees in electronic engineering from Keio University, Kanagawa, Japan, in 1972 and 1974, respectively.

In 1974, he joined NTT Electrical Communication Laboratory, Tokyo, Japan. He initially did research and development work on CMOS digital and analog LSI's for communication use. He also worked in high-frequency analog IC's for satellite and optical communication systems. In 1989, he was transferred to the NTT Electronics Technology Corporation, Tokyo, Japan, where he is involved in the development of broadband GaAs analog IC's and modules.

Mr. Kikuchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Yuhki Imai (M'92) was born in Tokyo, Japan, in 1955. He received the B.S., M.E., and Dr. Eng. degrees in applied physics from Waseda University in 1977, 1979, and 1991, respectively.

In 1979 he joined the NTT Electrical Communication Laboratories. He has been engaged in the research of microwave GaAs and InP MESFET fabrication technologies, low-current GaAs MMIC design for mobile communications, and high-speed GaAs IC design for 10Gb/s lightwave communications. He is now engaged in the research of future very high-speed IC design using GaAs and InP-based devices.

Dr. Imai is a member of the Institute of Electronics, Information and Communication Engineers of Japan.